Listing of the Claims:

The following list provides the current status of the claims in the present application:

1-44. (Cancelled)

45. (Previously presented) A memory device, comprising:

a first memory array having a cell plate and memory cells;

a second memory array having a cell plate and memory cells;

a plurality of sense amplifiers, each coupled to a respective first digit line coupled to memory cells of the first memory array and further coupled to a respective second digit line coupled to memory cells of the second memory array;

a switch coupled to the cell plate of the first memory array and further coupled to the cell plate of the second memory array to electrically couple the cell plates of the respective memory arrays; the switch adapted to decouple the cell plates of the first and second memory arrays in response to an inactive balance signal; and

a control circuit coupled to the switch and adapted to generate an inactive balance signal when accessing a memory cell of the first or second memory array.

46. (Previously presented) The memory device of claim 45 wherein the first and second arrays are located adjacent to one another.

47. (Previously presented) The memory device of claim 45, further comprising a bias generator coupled to the cell plates of the first and second memory arrays to bias the cell plates to a reference voltage level.

48. (Previously presented) The memory device of claim 47 wherein the bias generator comprises a voltage generator adapted to generate an output voltage having a voltage level approximately half of a supply voltage level.

49. (Previously presented) The memory device of claim 45 wherein the switch coupled to the cell plates of the first and second memory arrays comprises a transistor having a first terminal coupled to the cell plate of the first memory array, a second terminal coupled to the cell plate of the second memory array, and a control terminal coupled to the control circuit.

50. (Previously presented) A memory device, comprising:

a first memory array formed in a first region of a substrate, the first memory array having memory cells;

a second memory array formed in a second region of the substrate, the second memory array having memory cells;

a plurality of sense amplifiers, each coupled to a respective first digit line coupled to memory cells of the first memory array and further coupled to a respective second digit line coupled to memory cells of the second memory array;

a switch coupled to the first region of the substrate and further coupled to the second region of the substrate to electrically couple the regions of the substrate of the respective memory arrays; the switch adapted to decouple the first and second regions of the substrate in response to an inactive balance signal; and

a control circuit coupled to the switch and adapted to generate an inactive balance signal when accessing a memory cell of the first or second memory array.

51. (Previously presented) The memory device of claim 50 wherein the first and second arrays are formed adjacent to one another.

52. (Previously presented) The memory device of claim 50, further comprising a bias generator coupled to the first and second regions of the substrate to bias the first and second regions to a reference voltage level.

53. (Previously presented) The memory device of claim 52 wherein the bias generator comprises a voltage generator adapted to generate an negative output voltage.

54. (Previously presented) The memory device of claim 50 wherein the switch coupled to the first and second regions of the substrate comprises a transistor having a first terminal coupled to the first region of the substrate, a second terminal coupled to the second region of the substrate, and a control terminal coupled to the control circuit.

55. (Previously presented) A memory device, comprising:

a first plurality of memory cell arrays, the first plurality having at least one cell plate for the memory cell arrays;

a second plurality of memory cell arrays, the second plurality having at least one cell plate for the memory cell arrays; the memory cell arrays of the first plurality located adjacent the memory cell arrays of the second plurality;

a plurality of sets of sense amplifiers, each set of sense amplifiers having sense amplifiers coupled to respective pairs of digit lines, a first digit line of each pair coupled to memory cells of a memory cell array in the first plurality of memory cell arrays and a second digit line of each pair coupled to memory cells of a memory cell array of the second plurality of memory cell arrays;

a switch coupled to the cell plate of the first plurality of memory cell arrays and further coupled to the cell plate of the second plurality of memory cell arrays to electrically couple together the cell plates of the first and second pluralities in response to an active switch signal and decouple the cell plates of the first and second pluralities in response to an inactive switch signal; and

a control circuit coupled to the switch and adapted to generate an active switch signal prior to initiation of a memory access operation to memory cells of the first plurality of memory cell arrays or memory cells of the second plurality of memory cell arrays and generate an inactive switch signal in response to the initiation of a memory access operation.

56. (Previously presented) The memory device of claim 55 wherein the first plurality of memory cell arrays are formed in a first region of a substrate and the second plurality of memory cell arrays are formed in a second region of the substrate, and the memory device comprises a second switch coupled to the first and second regions of the substrate to electrically couple together the first and second regions in response to an active switch signal and decouple the first and second regions in response to an inactive switch signal.

57. (Previously presented) The memory device of claim 55, further comprising a bias generator coupled to the cell plates of the first plurality of memory cell arrays and further coupled to the cell plates of the second plurality of memory cell arrays to bias the cell plates to a reference voltage level.

58. (Previously presented) The memory device of claim 57 wherein the bias generator comprises a voltage generator adapted to generate an output voltage having a voltage level approximately half of a supply voltage level.

59. (Previously presented) The memory device of claim 55 wherein the switch coupled to the cell plates of the first and second plurality of memory cell arrays comprises a transistor having a first terminal coupled to the cell plate of the first plurality of memory cell arrays, a second terminal coupled to the cell plate of the second plurality of memory cell arrays, and a control terminal coupled to the control circuit.

60. (Previously presented) A method for accessing dynamic random access memory cells, comprising:

biasing cell plates of adjacent memory cell arrays to a reference voltage level;

coupling the cell plates of the adjacent memory cell arrays prior to initiation of a memory access operation to a memory cell in either of the adjacent memory cell arrays;

decoupling the cell plates of the adjacent memory cell arrays in response to initiation of the memory access operation to a memory cell in either of the adjacent memory cell arrays; and

sensing a voltage differential between the accessed memory cell and the cell plate of the memory cell array in which the accessed memory cell is not located.

61. (Previously presented) The method of claim 60, further comprising

coupling respective regions of a substrate in which in which the adjacent memory cell arrays are formed prior to initiation of a memory access operation to a memory cell in either of the adjacent memory cell arrays; and

decoupling the respective regions of the substrate of the adjacent memory cell arrays in response to initiation of the memory access operation to a memory cell in either of the adjacent memory cell arrays.

62. (Previously presented) The method of claim 60 wherein biasing the cell plates of adjacent memory cell arrays comprises biasing the cell plates of adjacent memory cell arrays to a voltage level approximately half of a supply voltage level.

63. (Previously presented) The method of claim 60 wherein sensing a voltage differential between the accessed memory cell and the cell plate of the memory cell array in which the accessed memory cell is not located comprises activating a sense amplifier having an open digit line architecture coupled to a first digit line coupled to memory cells of one of the memory cell arrays and further coupled to a second digit line coupled to memory cells of the other memory cell array.

64. (Previously presented) A method for accessing dynamic random access memory, comprising:

electrically coupling together cell plates of first and second memory cell arrays;

decoupling the cell plates of the first and second memory cell arrays;

activating a row of memory cells in the first memory cell array; and

for at least one memory cell of the activated row, comparing a voltage resulting from activation of the row of memory cells and a reference voltage of the second memory cell array.

65. (Previously presented) The method of claim 64, further comprising biasing the cell plates of the first and second memory cell arrays to the reference voltage prior to decoupling the cell plates of the first and second memory cell arrays.

66. (Previously presented) The method of claim 65 wherein biasing the cell plates of the first and second memory cell arrays comprises biasing the cell plates of adjacent memory cell arrays to a voltage level approximately half of a supply voltage level.

67. (Previously presented) The method of claim 64, further comprising:

electrically coupling together respective regions of a substrate in which the first and second memory cell arrays are formed; and

decoupling the respective regions of the substrate in which the first and second memory cell arrays are formed prior to activating a row of memory cells in the first memory cell array.